IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant	:	Gary A Brist, et al	
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Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Declaration of John Travis Pursuant to 37 C.F.R. §1.131

Sir:

I, John Travis, hereby declare that:

1. I am a citizen of the United States.

2. I currently work as an attorney at Intel Corporation.

3. Between the dates of at least 6/21/2002 and 9/23/2002, I worked continuously as an attorney at the law firm Blakely, Sokoloff, Taylor & Zafman (BSTZ).

4. Subsequent to William Ryann leaving BSTZ, I was assigned the above captioned application according to standard firm procedures.

5. From assignment of the above captioned application ("the application") to the application filing on 9/23/2002, I pursued filing the application with reasonable diligence in view of my existing case load.

6. As evidence of assignment of the application and reasonable diligence in filing the application, attached hereto as Exhibit B is an email exchange with the inventors.

7. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified patent application or any patent issued thereon.

Executed on: 1-27-2006

By: John Travis

John Travis, Reg. No. 43,203

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

A LIMITED LIABILITY PARTNERSHIP INCLUDING LAW CORPORATIONS

ONE BARTON SKYWAY
1501 SOUTH MOPAC, SUITE 250
AUSTIN, TEXAS 78746
(512) 330-0844 TELEPHONE
(512) 330-0476 FAX

FACSIMILE TRANSMITTAL

TO: Teresa Edwards for Michael Bernadicou	FROM: Dionne Robinson for William Ryann
COMPANY: BSTZ	DATE: [redacted]
FAX NUMBER: SV	TOTAL NO. OF PAGES INCLUDING COVER: 35
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NOTES/COMMENTS:

P12136

18957

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TMG INVENTION DISCLOSURE

Located at: http://legal.intel.com

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LEGAL ID# ____________(legal dept. use only) DATE: ____________________

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically via e-mail to "invention disclosure submission" if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call **503-264-0444.**

Fill out the below and follow the instructions:

1. **Field of the Invention:**
   - ☐ **Semiconductor Process: device and integration**
   - ☐ **Semiconductor Process + Equipment: thin films**
   - ☐ **Semiconductor Process + Equipment: etch/litho**
   - ☐ **Circuit Design**
   - ☐ **Flash**
   - ☐ **Test**
   - ☐ **CQN (Q&R)**
   - ☐ **Packaging**
   - X **Boards/Cartridge**
   - ☐ **Automation**
   - ☐ **Other**

2. **Concise Title of Invention:**

   Selectively defined diffusion layer on metal using lasers

3. **<u>Brief</u> Description of Invention (<u>please use only space provided</u> and font #10 or larger. Write the Key Elements of the Invention):**

   The invention is:
   Method for developing a selectively defined diffusion layer on a metal surface by laser processing of a material layer at the metal surface.

   The key elements are:
   - **Use of material layer on the metal surface as source of doping elements/compounds.**
   - **Use of laser energy to make doping elements within the material available for diffusion.**
   - **Use of photothermal laser energy produced in laser ablation to diffuse elements from the material layer into the metal surface.**

RECEIVED

[redacted]

PATENT DATABASE GROUP
INTEL LEGAL TEAM

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4. Inventor(s):

Name:Gary Brist
E-Mail Address:
gary.a.brist@intel.com

WWID#
10645854

M/S:
AG4-409

Phone:
503-456-1246

Fax:
503-456-1224

Home Address:
8300 NE HWY 240
Yamhill, OR 97148

Citizenship:
USA

Supervisor Name:
Mike C. Garner

Supervisor Phone:
480-765-2588

Supervisor M/S:
SC11-230

Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR___
STTD___ CQN___
SMTD____TCAD___
Other?___MTO________

Contractor:
YES _______
NO __XX_____

Inventor Signature:

Name: Gary Long
E-Mail Address:
Gary.b.long@intel.com

WWID#
~~10646016~~ 10646106

M/S:
AG4-409

Phone:
503-456-1308

Fax:
503-456-1224

Home Address:
6778 SW 174th
Aloha, OR 97007

Citizenship:
US

Supervisor Name:
Tom Hudson

Supervisor Phone:
8-554-6051

Supervisor M/S:
CH7-302

Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR___
STTD___ CQN___
SMTD____TCAD___
Other?__CSMO_______

Contractor:
YES _______
NO ___X____

Inventor Signature:

Name:
Daryl Sato
E-Mail Address:
Daryl.a.sato@intel.com

WWID#
10632810

M/S:
AG4-409

Phone:
503-456-1310

Fax:
503-456-1224

Home Address:
17230 NW Lone Rock Lane
Beaverton, OR 97006

Citizenship:
US

Supervisor Name:
Tom Hudson

Supervisor Phone:
8-554-6051

Supervisor M/S:
CH7-302

Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR___
STTD___ CQN___
SMTD____TCAD___
Other?__CSMO_______

Contractor:
YES _______
NO __XX___

Inventor Signature:

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

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5. HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)

DATE: ____________________ SUPERVISOR NAME: ______________________________

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?
If yes, explain and give date:
(Give expected tape out date if applicable):

7. Has the subject matter of present disclosure been published or will it be published outside of Intel? NO
If yes, explain and give date:

8. Has a product using or manufactured using the present disclosure been sold or offered for sale?
If yes, explain and give date: NO

9. Has this invention been conceived, or constructed during accomplishment of a government or third party contract? NO If yes, give contract name and number:

10. Explain the problem being addressed by the invention:

Selective altering of metal properties through diffusion of secondary material into the metal.

11. Explain current state of the art (i.e, how the problem is solved today):

Presently the problem described above is solved by:

12. Explain technical advantages of the invention over current state of the art:

A selective diffusion region can result in a region with different electrical, mechanical, and/or chemical properties. By selectively altering the chemical properties, the diffusion region can be used as an etch resist. By selectively altering the electrical properties, resistive or magnetic regions could be selectively developed onto a metal layer.

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13. a. Is the invention experimentally verified?
 b. Is the invention verified with simulation?
 c. If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):

It has also been observed, that during some processes of CO2 laser ablation (laser drilling of uVias) through FR4, and other epoxy resins used in making circuit boards, that the copper foil at the bottom of an ablated uvia has been selectively changed and etches at a slower rate. Cross section analysis of vias from this process prior to etching indicated that an area within the uvia on the Cu foil surface had flowed/melted. No composition analysis of the flowed/melted surface has been done at this time; but, it is believed that during the laser process of ablating the via that elements, either Cu oxide from the black oxide treatment layer or elements present within the ablated via generated from the breakdown of the resin and glass within the FR4 material, mixed or diffused within the Cu at the foil surface.

Note1: The ability of the laser to heat the Cu foil is increased in the case of a laminated circuit board due to the black oxide treatment of the foil prior to lamination for improve bond strength. This black oxide has a rougher surface then Cu foil and has an increased absorption of laser energy.

Note2: It has also been understood that elements present within protective coatings used on Cu foil, such as Chrome, diffuse into the Cu foil during lamination cycles. In the case of Teflon laminates, with lamination temperatures (~360-390C), a Chromate layer on the surface of the Cu foil that alters the etch rate of the Cu foil is developed. This chromate layer is considerably thicker in Teflon laminate foils than in standard epoxy laminate foils created with lower lamination temperatures. On 1oz Cu foil, the etch rate difference is ~25% as observed in PCB etch tests. Using thinner foils, this rate would be greater and allow for its use as an etch resist.

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14. **Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):**

1. Material containing elements/compounds that will be diffused into the metal is coated/laminated/placed on the metal surface. The elements/compounds to be diffused can be either elemental, part of a polymer chain, or part of a material composite.
2. Laser energy is used to reduce the material into constituent elements/compounds.
3. As the ablation depth reaches the metal surface, the laser energy heats the metal while elements/compounds are still present from ablation of material at the metal surface. As the laser energy continues some of the elements/compounds present diffuse into the metal
4. Once the bulk of the elements/compounds are removed/ejected from the ablated opening, the laser energy can be tuned to continue/maintain heating of the metal to advance the diffusion.
5. The ability of the diffusion may be related to the depth/aspect ratio of the ablated opening, to the energy absorption rate of the metal and pulse waveform and wavelength of the laser.

Referenced sketches/dwg's /diagrams: (use additional page(s))

15.

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Drawings (use as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)

Figure 1. Present State of the Art (often this is helpful to explain your invention, but it is not required).

Figure 2. The Invention (use additional figures as needed to show details and additional embodiments)

- Creation of a selective diffusion layer on metal using laser ablation of a coating layer

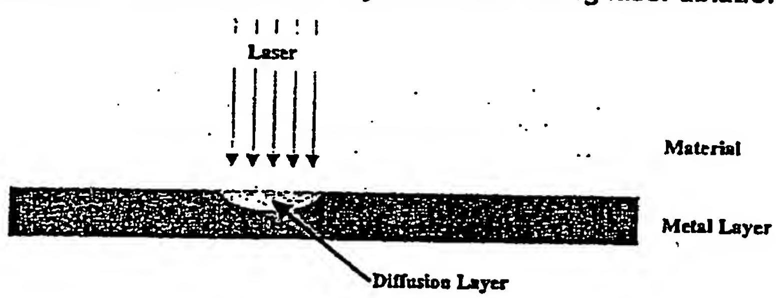
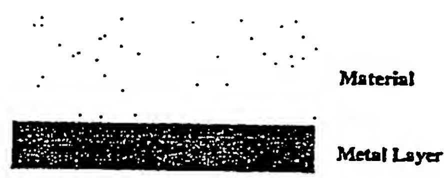
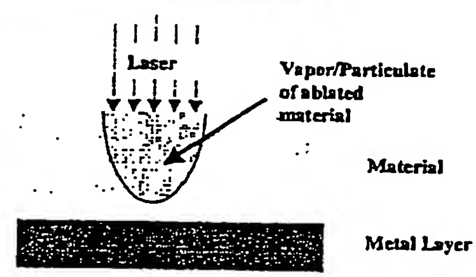


Figure 3,4,5, etc. Steps for Making Invention

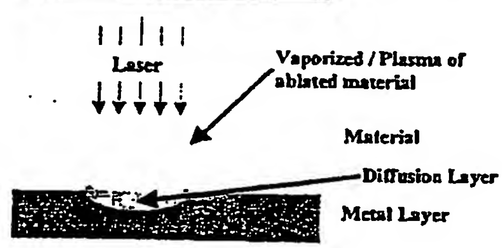
Step1: Coating metal layer with selected material



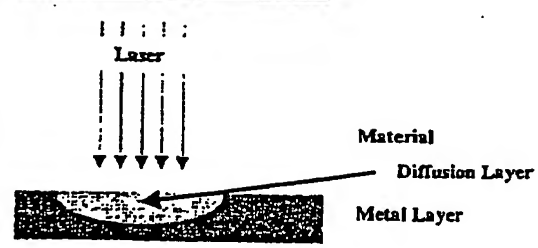
Step2: Laser to ablate material layer into vapor/cloud of particulates.



Step3: Photothermal energy / heating of metal layer in presence of particulates from material ablation initiates diffusion of some particulates into metal layer.



Step4: Continued control of laser energy after material ablation completes allows for further control of diffusion region.



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16. Key Supporting Data (1 page limit on separate page):

17. What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.): Printed circuit boards, packaging.

18. Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name: ______________________

19. Any other information IP committee should consider?

MENTOR REVIEW

If you don't already have a departmental peer review process for invention disclosures, we recommend you have it reviewed by a Mentor before you send your invention disclosure to Intel Legal. The purpose of this Mentor review is to ensure that the invention disclosure is written clearly enough for the IP Committee to comprehend your invention including all the novel aspects of it. Please refer to the list below for recommended Mentors by area. Select ONE Mentor to review and acknowledge. This recommended step is not meant to unreasonably slow down the invention disclosure process. If your Mentor fails to respond to you in a reasonable amount of time, then send your invention disclosure directly to Intel Legal.

AREA	MENTOR
Semiconductor Process – device and integration	Mark Bohr, Robert Chau, Krishna Seshan
Semiconductor Process – thin films	Ken Cadien, Chien Chiang
Semiconductor Process – etch/litho	Peter Silverman, Peter Charvat (etch), Yan Borodovsky (litho)
Circuit Design	Ian Young, Greg Taylor, Clair Webb, Rajesh Galivanche
Flash	Manzur Gill, Krishna Seshan
Test	J.J. Grealish, Rajesh Galivanche, Mike Mayberry
CQN (Q&R)	Ian Young, Greg Taylor, Clair Webb, Valluri (Bob) Rao
Packaging	Ken Kinsman, Bob Sankman, Rama Shukula
Boards/Cartridge	Leslie Polaski, J.J. Grealish
Automation	Sunit Rikhi
Optical and MEMS	Valluri (Bob) Rao
Legal Dept. Patent Attorneys	Ray Werner, Rob Winkle, John Greaves, Wayne Rupert

DRAFT

UNITED STATES PATENT APPLICATION

PHOTO-THERMAL INDUCED DIFFUSION

Inventors:

Gary A. Brist
Gary B. Long
Daryl A. Sato

prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
512.330.0844

Attorney Docket No.: 42P12136

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PHOTO-THERMAL INDUCED DIFFUSION

BACKGROUND

[0001] The present invention relates to doping or diffusion of one material into another. In particular, the present invention relates to diffusion of a portion of a material into another in semiconductor package substrate and related processing.

BACKGROUND OF THE RELATED ART

[0002] In the fabrication of microchips or semiconductor dice, semiconductor wafers are processed and sliced into individual dice. The dice may then be used in a wide variety of devices. For example, a die may be used in an electronic device by being electronically coupled to a printed circuit board (PCB) of the device.

[0003] Forming a die generally involves depositing layers of varying purposes. For example, an inter-layer dielectric (ILD) may be deposited and patterned to isolate conductive circuit features. The circuitry of the die is made up of layers of such features.

[0004] Once the die is formed, packaging will take place. The packaging process involves the coupling of the die to a protective package substrate which in turn couples directly to the PCB. The package substrate includes bond pads which are coupled to an array of metal bumps or other conductive features of the compact die. The bond pads are in turn coupled to internal circuitry of the package substrate. In this manner, the larger package substrate acts as an electronic interface to fan out electronic paths between the compact internal circuitry of the die to the much larger PCB.

[0005] Similar to die formation, package substrate processing may include forming the above-indicated internal circuitry of the package substrate. Again, such internal circuitry may include multiple layers of circuit features. Similar to die circuit features,

package substrate circuit features may include metal traces isolated by ILD. In order to form layers of internal circuitry in the package substrate, a time consuming multi-step process of deposition and photolithographic patterning and developing is generally employed as described below.

[0006] Initially, a metal core for a package substrate may be provided having a protective coating thereon. The protective coating may be a conventional organic material to prevent oxidation of the metal core or a metal layer on the metal core prior to processing. The core may undergo initial processing, such as via formation prior to the addition of layers of circuitry. The protective coating may then be chemically removed, followed by deposition of silicon based dielectric material layers to support layers of circuitry noted above. The silicon based dielectric material layer deposition may include the formation of an etch stop layer followed by the formation of ILD material layers.

[0007] Metal traces or other circuit features may be patterned into, and isolated by, the dielectric material. This may be achieved by photolithographic patterning and developing. First, a resist layer is placed above the dielectric material. The resist layer may be of photosensitive material and exposed to a photomasking tool. The photomasking tool is specially configured to deliver a pattern of light energy, such as ultraviolet light, to the resist layer, thereby selectively removing portions of the resist in accordance with the pattern of light energy. Subsequently, a chemical developer may be delivered to the package substrate, etching trenches into the dielectric material, at locations where it is not protected by resist material (i.e. where the resist has been removed by the photomasking tool). This may be followed by metalization, wherein metal lines or other circuit features are formed in the trenches, for example by conventional deposition techniques.

[0008] Unfortunately, a high cost is incurred and throughput limited by the time consuming process described above. Furthermore, material expenses are incurred by the need for a host of materials, such as those indicated above, in order to form even a single metal circuit feature of a single circuit layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Fig. 1 is a side sectional view of a photo-thermal apparatus directing a photo-thermal energy to a substrate including a first material adjacent a second material.

[0010] Fig. 2 is an exploded view of section 2-2 taken from Fig. 1 revealing the photo-thermal energy applied to the substrate.

[0011] Fig. 3A is side cross sectional view of a package substrate including diffusion layers adjacent metal layers.

[0012] Fig. 3B is a side cross sectional view of the package substrate of Fig. 3A having portions of the diffusion layers diffused into the metal layers to form metal traces.

[0013] Fig. 3C is a side cross sectional view of the package substrate of Fig. 3B with diffusion layers removed.

[0014] Fig. 3D is a side cross sectional view of the package substrate of Fig. 3C with metal layers removed.

[0015] Fig. 4 is a side cross sectional view of a package substrate having metal traces formed by diffusion of a portion of one material into another and isolated by inter-layer dielectric (ILD) material.

[0016] Fig. 5 is a side cross sectional view of a semiconductor package utilizing the package substrate of Fig. 4.

[0017] Fig. 6 is a flow chart summarizing embodiments of forming a semiconductor package with metal traces formed by diffusion of a portion of one material into another.

DETAILED DESCRIPTION

[0018] Methods of diffusing a portion of a first material into a second material are described. Aspects of embodiments are described and illustrated by the accompanying drawings. While the following embodiments are described with reference to a particular method of forming metal traces in a package substrate, the embodiments are applicable to any diffusion or doping of one material into another. This may include any method of photo-thermal induced diffusion including for processing of a package or semiconductor substrate.

[0019] Referring now to Fig. 1, a photo-thermal apparatus is shown in the form of an yttrium aluminum garnate (YAG) laser device 150. The YAG laser device 150 includes a total reflection mirror 151 and a partial reflection mirror 152 with a laser cavity 155 therebetween. An amplifying medium 165 is positioned in the laser cavity 155.

[0020] A power source 158 is coupled to the YAG laser device 150 to power a light source to repeatedly direct light 160 through the amplifying medium 165 as described further below. The amplifying medium 165 includes a rod of yttrium aluminum garnate providing ions of lanthanide metal neodymium. The light 160 is energized and reenergized by the amplifying medium 165 as it repeatedly passes there through. As the light 160 encounters the total reflection mirror 151 it is reflected back through the amplifying medium 165 and toward the partial reflection mirror 152. Generally, the light 160 is also reflected by the partial reflection mirror 152 back through the

amplifying medium 165. However, between about 1% and about 3% of the light 160 passes beyond the partial reflection mirror 152 in the form of a laser 100.

[0021] The laser 100 shown in Fig. 1 is directed at a substrate 175 which includes a first material 177 adjacent a second material 179. The materials 177, 179 may be in the form of layers of the substrate 175. As the laser 100 encounters the substrate 175 a portion of the first material 177 is diffused into the second material 179 as described further below.

[0022] In one embodiment the substrate 175 is a package substrate to accommodate a semiconductor die. Examples of such embodiments are described further herein with reference to Figs. 3A-5. Additionally, however, any substrate including a first material 177 adjacent a second material 179 may be subjected to a laser 100 or other form of photo-thermal energy for diffusion of a portion of the first material 177 into the second material 179. This may include semiconductor substrates, and substrates for printed circuit boards (PCBs).

[0023] Referring to Fig. 2, an exploded view of section 2-2 taken from Fig. 1 is shown. The laser 100 can be seen penetrating the first material 177 of the substrate 175. In the embodiment shown, the laser 100 actually penetrates the substrate 175 to a point beyond the first material 177. However, this is not required to achieve diffusion into the second material 179 as described below. This is because heat from the laser 100 will penetrate beyond the terminating point of the laser 100.

[0024] As the laser 100 contacts the substrate 175 a portion of the first material 177 is heated and diffused into the second material 179 to form a combined material portion 225 of the substrate 175. For example, in one embodiment where the materials 177, 179 are different metals, the combined material portion 225 may be an alloy made up of the different materials 177, 179. As shown in Fig. 2, some of the first particles 176 of

the first material 177 can be seen in the combined material portion 225 along with second particles 178 of the second material 179. As also shown in Fig. 2, the combined material portion 225 may extend above the second material 179.

[0025] With reference to Figs. 1 and 2, the formation of a combined material portion 225 by diffusion of a portion of a first material 177 into a second material 179 with a photo-thermal source of energy, such as a laser 100, is shown. A wide range of parameters are available to choose from in forming such a combined material portion 225. For example, a variety of choices are available regarding the size, type, strength, and duration of the photo-thermal source of energy, as well the forms and types of materials 177, 179 and substrates 175. With reference to Figs. 3A-3D particular embodiments of forming combined material portions in the form of metal traces 325 for a package substrate 375 are described. However, as noted above, a host of other applications may employ embodiments of the described diffusion or doping techniques. Additionally, the selective diffusion described may be used to configure a combined material portion 225 having particular electrical, mechanical or chemical properties, one such example described below with reference to Figs. 3A-5.

[0026] Referring now to Figs. 3A-3D, an embodiment of a package substrate 375 is shown where metal traces 325 are employed. The package substrate 375 may be for a semiconductor package, such as the semiconductor package 500 shown in Fig. 5. The package substrate 375 may include a core 376 made up of a ceramic, fiber-reinforced epoxy, copper clad, or other conventional material.

[0027] As described below, and with reference to Fig. 6, metal layers 379 may be initially formed on the core 376 as shown at block 610. Fig. 6 is a flow-chart summarizing embodiments of forming package substrates and semiconductor packages employing metal traces formed by photo-thermal induced diffusion. Fig. 6 is

referenced throughout the remainder of the description as an aid in explaining these embodiments.

[0028] The metal layers 379 noted above may be formed on the core 376 by conventional metalization techniques. For example, in one embodiment, the core 376 is placed in a metalization reactor which may be a conventional plasma enhanced chemical vapor deposition (PECVD) apparatus. The reactor may be activated to energize a vapor of metal to a plasma state for deposition on the core 376. The metalization may proceed at conventional pressures, temperatures, RF, and power. For example, in one embodiment, pressure within the reactor is maintained between about 2.0 Torr and about 10.00 Torr, a temperature of between about 250°C and about 450°C maintained, RF maintained at standard frequencies, and between about 1,600 watts and about 1,800 watts supplied.

[0029] The metal layer 379 deposited may be of a metal chosen depending upon the type of metal traces 325 to be formed as described further herein. For example, in an embodiment where the metal traces 325 are configured to be copper based, the metal layer 379 is of copper. Additionally, the metal layer 379 may be between about 5 and about 20 microns in thickness.

[0030] Continuing with reference to Fig. 3A, a diffusion layer 377 is present above the metal layer 379. The diffusion layer 377 includes a material selected for diffusion into the metal layer 379 as described with reference to Figs. 1 and 2. For example, the diffusion layer 377 may include tin for diffusion into the metal layer 379 to form copper tin metal traces 325 as described further herein with reference to Fig. 3B.

[0031] The diffusion layer 377 may also include materials selected to protect the metal layer 379. For example, in one embodiment, the diffusion layer 377 acts as a conversion coating to prevent oxidation of the underlying metal layer 379. The

conversion coating materials may be conventional organic materials commonly used to form surface coatings. For example, the diffusion layer 377 may include a conventional polymer epoxy, possibly with added nitrogen or bromine groups. Additionally, the diffusion layer may be an organic metal, such as a polymer with tin side groups as tin may bond with carbon. Alternatively, in another embodiment, tin may be independently dispersed within the organic material of the diffusion layer 377. Such organic materials generally form an adequate sealant to prevent oxidation as indicated.

[0032] The diffusion layer 377 may be applied to the metal layer 379, as indicated at block 620 of Fig. 6, in liquid form by conventional syringe delivery and dried. Additionally, the diffusion layer 377 may be between about 0.01 and about 0.50 microns. As described further below, the thickness of the diffusion layer 377 may be determined based on the amount of material to be diffused into the metal layer 379 in forming the metal traces 325 (as shown in Fig. 3B).

[0033] Continuing with reference to Fig. 3A, a pattern of vias 350 are shown formed in the package substrate 375 as referenced at block 630 of Fig. 6. Vias 350 allow for the formation of interconnecting electrical paths across the core 376 such that a functional package substrate 375 may be formed. The vias 350 may be formed by laser drilling, machine punching, or other conventional means. The particular placement and configuration of the vias 350 is a matter of design choice depending upon the circuit design to be employed by the package substrate 375.

[0034] Referring to Fig. 3B, the package substrate of Fig. 3A is shown with a pattern of metal traces 325. As described further here, the metal traces 325 are formed in the manner that the combined material portions 225 of Fig. 2 are formed. That is, as shown at block 640 of Fig. 6, a photo-thermal energy is applied to at least the diffusion

layer 377 at the locations of the metal traces 325 to diffuse material from the diffusion layer 377 into the metal layer 379, forming the metal traces 325 thereat. The metal traces 325 are of a particular alloy as described below. The alloy may be configured to be of particular chemical, electrical, and mechanical properties.

[0035] In one embodiment a YAG laser device is employed similar to that described with reference to Figs. 1 and 2. The YAG laser device directs a laser at the diffusion layer 377 in locations where the metal traces 325 are to be formed. In one embodiment, the size of the laser is from about 2 mils to about 8 mils. However, the exact size of the laser employed is a matter of design choice. In fact, most of the particular parameters of the laser will be a matter of design choice depending on a host of factors such as those noted below.

[0036] A variety of parameters may be considered during application of the laser as indicated above. For example, the size of the laser applied may depend upon, for example, the width of the metal traces 325 to be formed. Additionally, the laser may be applied for a time sufficient to fully diffuse portions of the diffusion layer 377 at the locations of the metal traces 325 into the metal layer 379. However, this amount of time is a matter of design choice depending upon, for example, the thickness of the diffusion layer 377 at these locations and the strength of the laser selected. Additionally, to ensure that metal traces 325 do not exceed an intended size, the laser may be applied for a set time at each location, regardless of any remaining portions of the diffusion layer 377 thereat.

[0037] In one embodiment, application of the laser to the package substrate 375 as described results in the diffusion of tin into the copper metal layer 375 forming metal traces 325 of a copper tin alloy. That is, the laser heats the diffusion layer 377 and at least a portion of the metal layer 379. The diffusion layer 277 is broken up in a manner

that allows diffusion of tin into the heated portion of the metal layer 379. At the same time depending on the particular make-up of the diffusion layer 377, other materials such as oxygen, carbon dioxide, nitrogen or other gas formations may be formed and dissipate away from the forming metal traces 325 of the package substrate 375.

[0038] As described above, the metal traces 325 are formed by application of a photo-thermal energy in the form of a laser as provided by a YAG laser device. However, this is not required. Other forms of photo-thermal energy may be used to direct a portion of the diffusion layer 377 into the metal layer 379 to form metal traces 325. For example, a CO_2 or infrared laser device may be employed to diffuse a portion of the diffusion layer 377 into the metal layer.

[0039] The particular pattern of metal traces 325 formed is again a matter of design choice. As with the placement and configuration of vias 350 described above, the pattern of metal traces 325 depends upon the overall circuit design to be displayed by the package substrate 375. As described above, the metal traces 325 are formed by diffusion as directed by a YAG laser device (such as that of Fig. 1). Therefore, the YAG laser device may be programmed to direct a laser to pattern the metal traces 325 in accordance with the circuit design of the package substrate 375.

[0040] Continuing with reference to Figs. 3B and 3C, along with Fig. 6, the remainder of the diffusion layer 377 is removed once the metal traces 325 are formed as shown at block 680. Removal of the diffusion layer 377 is achieved by application of etching or removal chemistry particularly configured to remove materials of the diffusion layer 377. For example, in the embodiment described above, the diffusion layer 377 may be of a conventional epoxy polymer having elements of tin incorporated therein. The epoxy polymer may be removed with conventional solvents during chemical mechanical polishing. For example, sodium hydroxide or alkaline strippers

may be used to remove the polymer. Additionally, such a stripper may be combined with an oxidizing fluoride solution to ensure removal of any excess tin of the diffusion layer 377. Once the diffusion layer 377 is removed, the package substrate 375 is washed with a conventional rinse or acid neutralizing solution to remove any excess solvents.

[0041] Referring to Figs. 3C and 3D, along with Fig. 6, the metal layer 379, with the exception of the metal traces 325 is removed as noted at block 660. In the embodiment described above, the metal layer 379 is of copper. Therefore, a removal chemistry including cupric chloride may be used to remove the remaining portions of the metal layer 379, leaving the core 376 with metal traces 325 of a copper tin alloy as shown in Fig. 3D. Once the metal layer 379 is completely removed, the package substrate 375 may again be washed with a conventional rinse or acid neutralizing solution to remove any excess cupric chloride.

[0042] In the above examples, the diffusion layer 377 and metal layer 379 are removed with removal chemistries which may have a minimal effect on the metal traces 325. For example, cupric chloride, while removing the metal layer 379, may also dissolve some of the alloy of the metal trace 325, but at only about 20-30% the dissolution rate of the metal layer 379. Therefore, in an embodiment where metal traces 325 are to have a thickness between about 10-15 microns and a width between about 20-30 microns, the metal traces 325 may actually be formed about 20-30% larger prior to removal of the diffusion 377 and metal 379 layers. For example, in such an embodiment, the metal traces 325 may be originally formed as indicated above with a thickness between 10-20 microns and a width between about 27-35 microns.

[0043] Continuing with reference to Fig. 3D, once metal traces 325 have been patterned above the core 376 as shown, subsequent processing my ensue by

conventional means. For example, the vias 350 may be filled with a conventional polymer epoxy material and repunched to accommodate interconnect features there through. That is, following formation of a new via lined with epoxy, interconnect material such as copper may be deposited therein by conventional means. Additionally, inter-layer dielectric (ILD) material may be deposited between the metal traces 325 as shown at block 670 of Fig. 6. Other circuit features and layers may also be provided above the metal traces 325 by conventional means as shown in Fig. 4.

[0044] Referring to Fig. 4, a package substrate 475 formed according to the methods described above with reference to Figs. 3A-3D is shown. In particular, a core 476 is shown accommodating metal trace layers 479 with metal traces 425 isolated by ILD material 480. Once the metal traces 425 are formed as indicated above, the package substrate 475 may be placed in a conventional PECVD apparatus for ILD deposition. The deposition may proceed at conventional pressures, temperatures, RF, and power. Once the metal trace layers 479 are complete, they may be planarized by conventional chemical mechanical polishing (CMP) techniques to leave surfaces of the metal traces 425 exposed for electrical connection to subsequently deposited circuit layers 430. The circuit layers 430 formed as indicated at block 680 of Fig. 6, may be of multi-layered circuitry having circuit features isolated by ILD material. The particular configuration of each circuit layer 430 may again be a matter of design choice.

[0045] Referring to Fig. 5, the package substrate 475 of Fig. 4 is shown as part of a completed semiconductor package 500. In the embodiment shown, bond pads 515 are shown electrically coupled to a circuit layer 430 and to metal bumps 516 of a die 520. The die 520 is secured to the package substrate 475 by a conventional adhesive underfill material 510. Conventional soldering techniques may be employed to couple the bond pads 515 to the circuit layer 430 and metal bumps 516. Similarly,

conventional reflow techniques may be used to cure the underfill material 510 and couple the die 510 to the package substrate 475 as indicated at block 690 of Fig. 6 to complete the semiconductor package 500.

[0046] Fig. 6 is a flow chart summarizing embodiments of forming metal traces as described above with reference to Figs. 3A-5. Namely, a photo-thermal energy is applied to a package substrate to form a pattern of metal traces as shown at block 640. This same package substrate may be coupled to a die to form a semiconductor package as shown at block 690.

[0047] Forming metal traces as indicated above increases throughput and may eliminate the need for a time-consuming photolithographic process. Additionally, material expenses are reduced as the formation of purely sacrificial layers of a substrate may be avoided. Furthermore, with respect to package substrates, the diffusion layer may be a conversion coating to prevent oxidation, as is often provided on package substrates, but having incorporated therein additional material for diffusion into an underlying material.

[0048] Embodiments described above include methods of inducing diffusion of one material into another by photo-thermal induction. Additionally, embodiments include reference to particular circuit features such as metal traces. Although exemplary embodiments describe particular methods of photo-thermal diffusion regarding package substrates, additional embodiments are possible. For example, techniques described may be applied to semiconductor substrates for PCBs, or other multilayered substrates. Additionally, diffusion into a material may be achieved by melting a portion of a metal in foil form above the material by a photo-thermal energy source. Furthermore, many changes, modifications, and substitutions may be made without departing from the spirit and scope of these embodiments.

CLAIMS

We Claim:

1. A method comprising applying a photo-thermal energy to a substrate having a first material adjacent a second material for diffusing a portion of the first material into the second material.

2. The method of claim 1 wherein the photo-thermal energy is one of a YAG laser, a CO_2 laser, and an infrared laser.

3. The method of claim 1 wherein the first material is a diffusion layer having the portion for diffusing and the second material is a metal layer of a metal, the photo-thermal energy to penetrate at least into the diffusion layer such that the diffusing forms an electrically conductive metal trace of the portion for diffusing and the metal.

4. The method of claim 3 wherein the portion for diffusing is tin, the metal is copper, and the metal trace is of a copper tin alloy.

5. The method of claim 3 wherein the photo-thermal energy is a laser of between about 2 mils and about 8 mils.

6. The method of claim 3 further comprising:

removing the diffusion layer; and

removing the metal layer, leaving the metal trace.

7. The method of claim 6 wherein the diffusing forms a metal trace that is between about 20 % and about 30% larger prior to said removing of the diffusion layer and said removing of the metal layer.

8. The method of claim 6 wherein the substrate is a package substrate having a core with an initial via therethrough, the core to support the metal trace, the method further comprising:

filling the via with a polymer;

forming a new via through the polymer leaving the new via lined with the polymer; and

depositing interconnect material in the new via.

9. The method of claim 8 further comprising:

depositing inter-layer dielectric material to isolate the metal trace and form a metal trace layer.

10. The method of claim 9 further comprising:

planarizing the metal trace layer to ensure that a surface of the metal trace is exposed; and

electronically coupling the surface to a die to be secured to the package substrate to form a semiconductor package.

11. A method comprising:

forming a metal layer on a core; and

placing a diffusion layer on the metal layer, the diffusion layer including a material for diffusing into the metal layer upon photo-thermal induction.

12. The method of claim 11 wherein the diffusion layer includes a conversion coating material to protect the metal layer from oxidation.

13. A substrate comprising:

a first material adjacent a second material; and

a combined material portion adjacent said first and second materials and resulting from application of a photo-thermal energy to at least the first material to diffuse a portion thereof into the second material to form the combined material portion.

14. The substrate of claim 13 for one of a semiconductor package, a printed circuit board and a die.

15. The substrate of claim 13 wherein said first material is in the form of a diffusion layer including the portion and said second material is in the form of a metal layer.

16. The substrate of claim 15 wherein the combined material portion is in the form of an electrically conductive metal trace.

17. The substrate of claim 16 wherein the metal trace is a copper tin alloy.

18. The substrate of claim 16 wherein the metal trace is between about 10 microns and about 20 microns in thickness and between about 27 microns and about 35 microns in width.

19. The substrate of claim 16 further comprising inter-layer dielectric material isolating the metal trace to form a metal trace layer.

20. A substrate comprising:

a metal layer; and

a diffusion layer on the metal layer and including a portion to diffuse into the metal layer upon photo-thermal induction.

21. The substrate of claim 20 wherein the metal layer is copper.

22. The substrate of claim 20 wherein the portion is tin.

23. The substrate of claim 20 wherein the diffusion layer includes an organic metal.

24. The substrate of claim 20 wherein the diffusion layer includes a conversion coating.

25. A system comprising:

a printed circuit board; and

a semiconductor package coupled to the printed circuit board and including a substrate with a metal trace formed by diffusion by photo-thermal induction of a portion of a first material into a second material.

26. The system of claim 25 wherein the metal trace is between about 10 microns and about 15 microns in thickness and between about 20 microns and about 30 microns in width.

ABSTRACT

Induction of diffusion by application of a photo-thermal energy. The diffusion may be of a portion of one material into another of a package substrate, semiconductor substrate, substrate for a printed circuit board (PCB) or other multi-layered substrate. The photo-thermal energy may be supplied by a YAG laser device, CO_2 laser device, or other energy source.

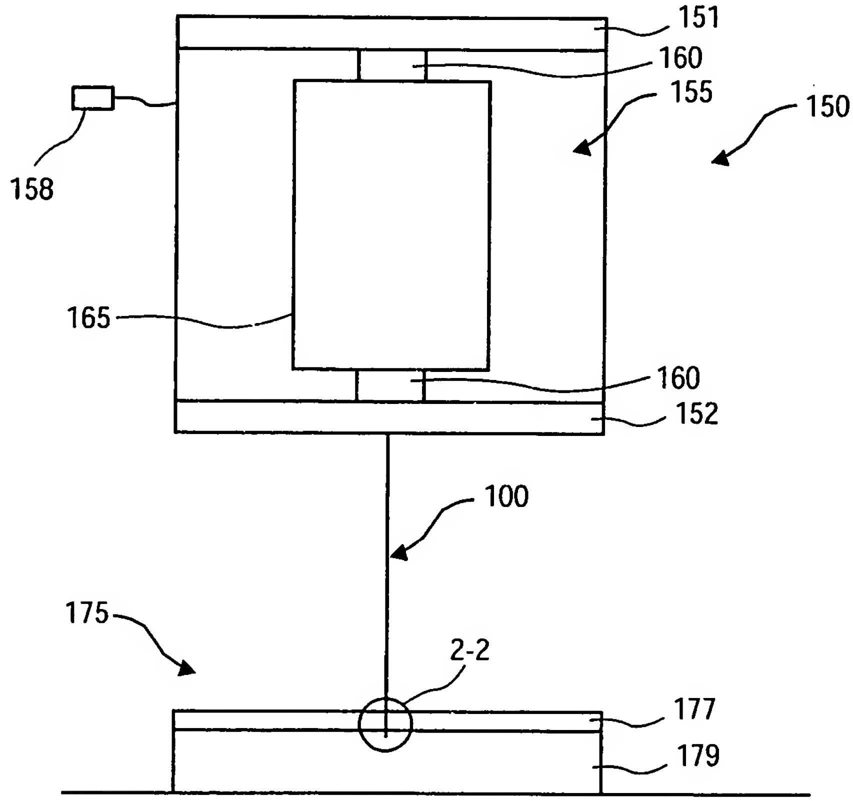

FIG. 1

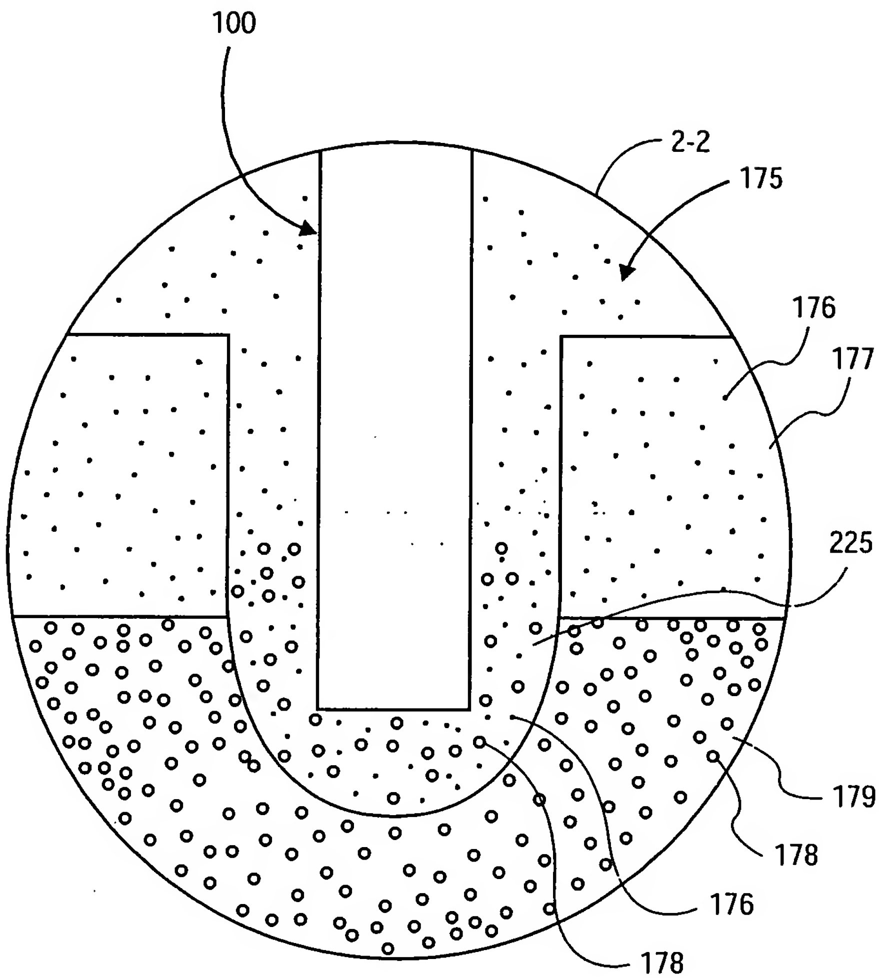

FIG. 2

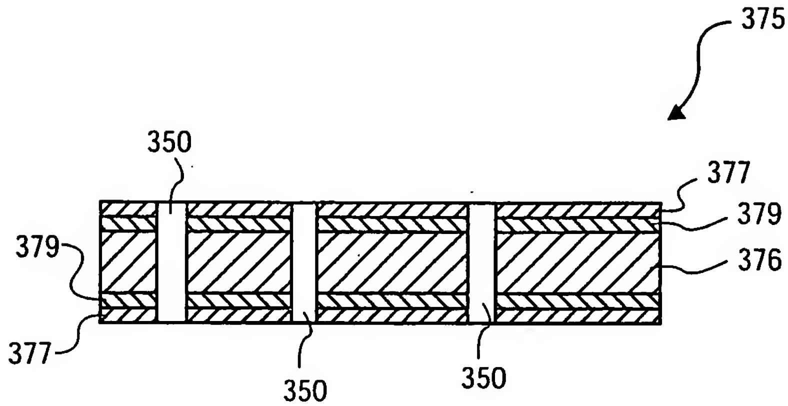
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FIG. 3A

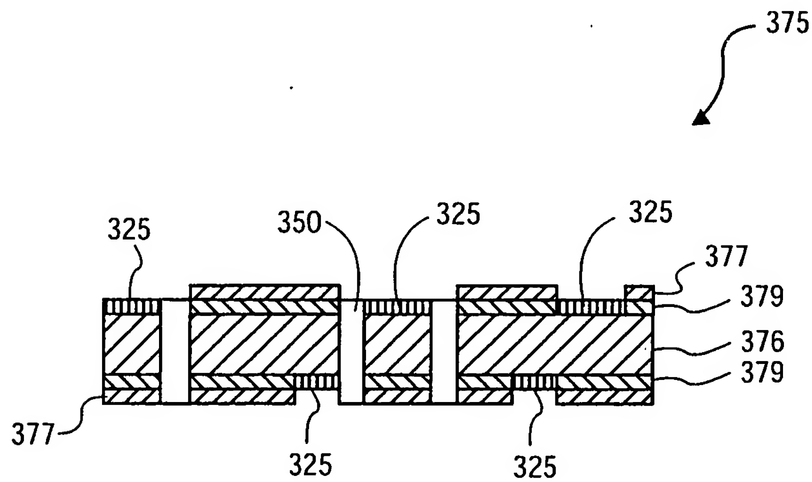
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FIG. 3B

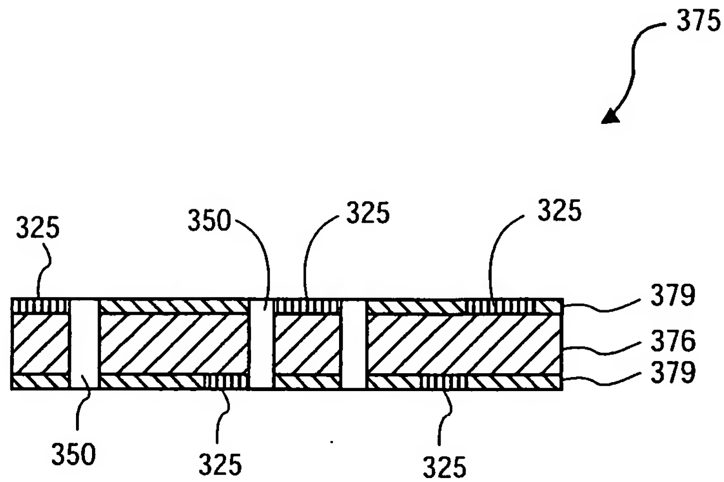
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FIG. 3C

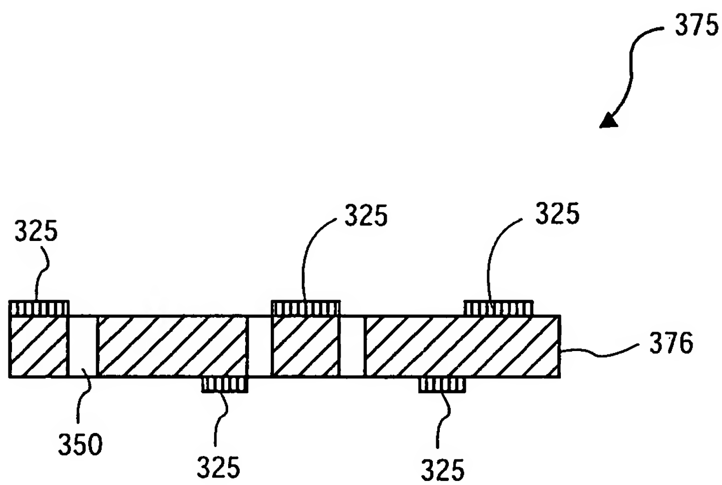
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FIG. 3D

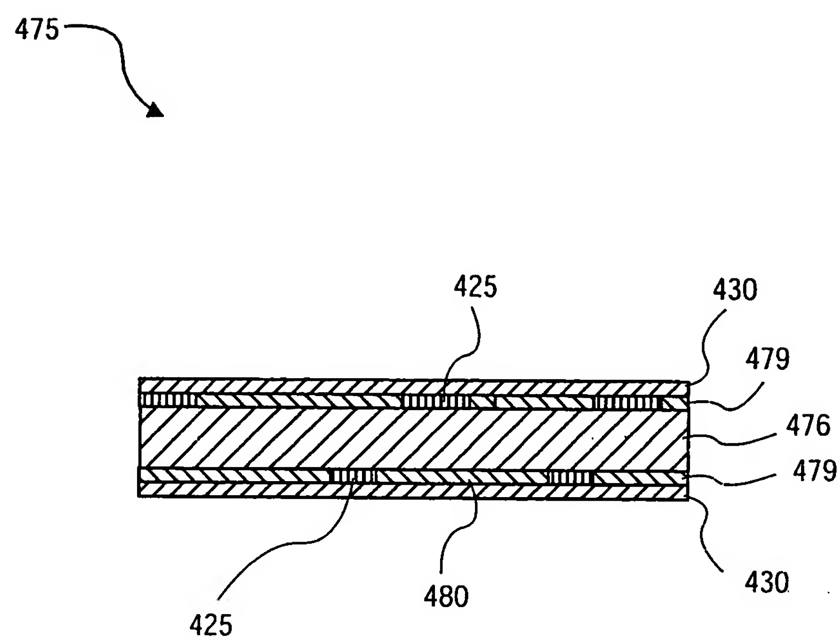

FIG. 4

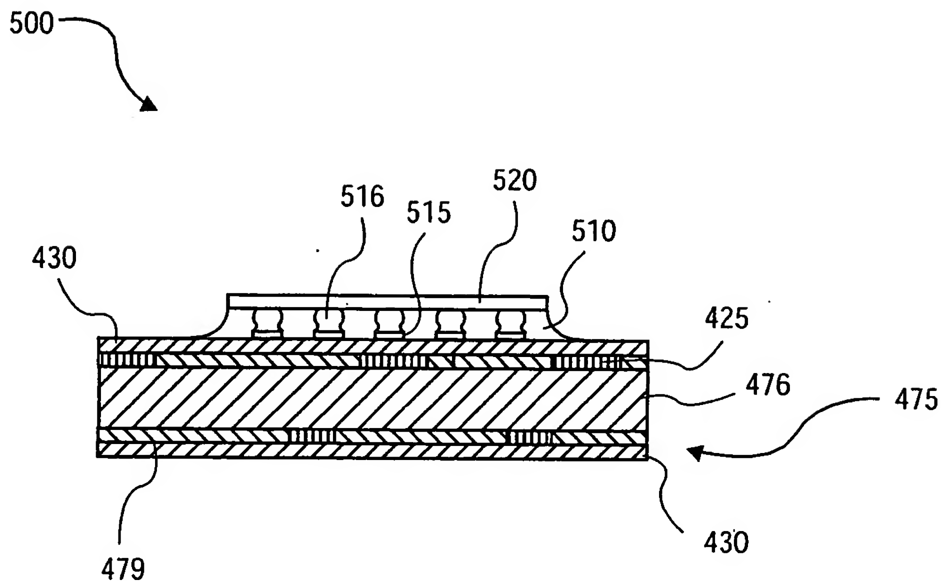

FIG. 5

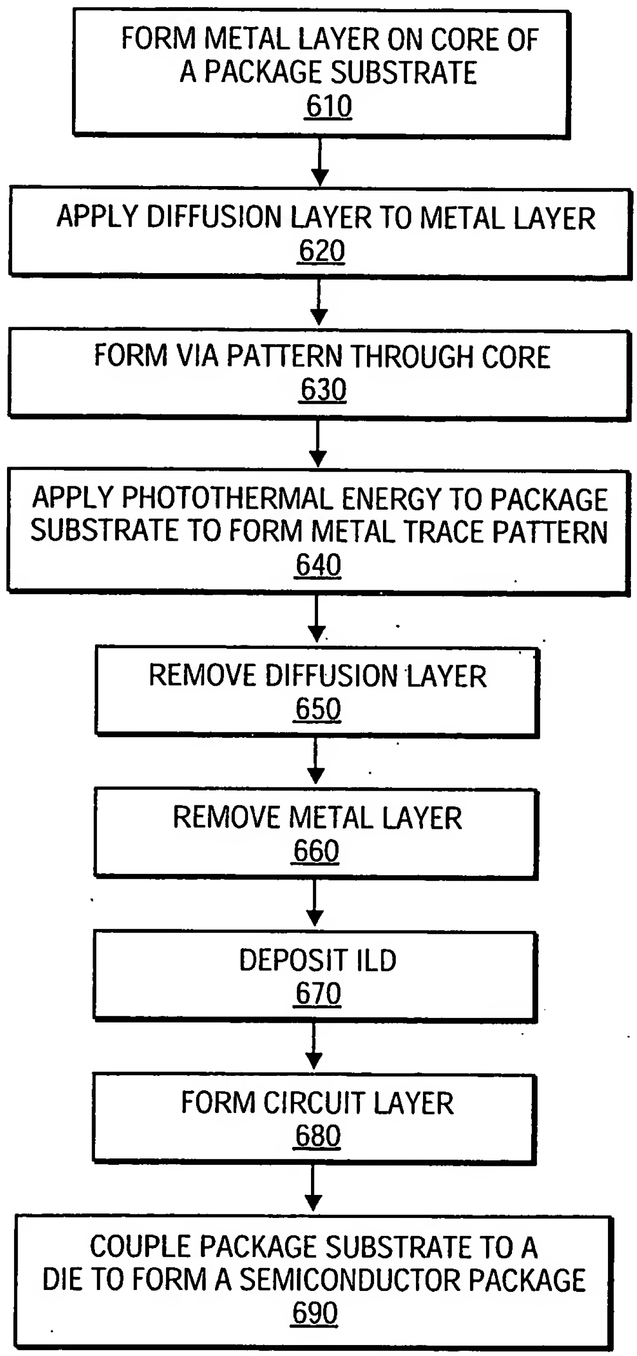
FORM METAL LAYER ON CORE OF A PACKAGE SUBSTRATE 610
APPLY DIFFUSION LAYER TO METAL LAYER 620
FORM VIA PATTERN THROUGH CORE 630
APPLY PHOTOTHERMAL ENERGY TO PACKAGE SUBSTRATE TO FORM METAL TRACE PATTERN 640
REMOVE DIFFUSION LAYER 650
REMOVE METAL LAYER 660
DEPOSIT ILD 670
FORM CIRCUIT LAYER 680
COUPLE PACKAGE SUBSTRATE TO A DIE TO FORM A SEMICONDUCTOR PACKAGE 690

FIG. 6

"Brist, Gary A" <gary.a.brist@intel.com>
09/12/02 11:22 AM

To: "'John_Travis@bstz.com'" <John_Travis@bstz.com>, "Brist, Gary A" <gary.a.brist@intel.com>, "Long, Gary B" <gary.b.long@intel.com>, "Sato, Daryl A" <daryl.a.sato@intel.com>
cc:
Subject: RE: Patent application P12136

John,

Application looks good. [redacted]

Gary Brist
PCB Technologist
Materials Technology Organization

MS: AG4-409
Phone: 503.456.1246
Fax: 503.456-1223
Email: gary.a.brist@intel.com

-----Original Message-----
From: John_Travis@bstz.com [mailto:John_Travis@bstz.com]
Sent: Friday, September 06, 2002 10:25 AM
To: gary.a.brist@intel.com; gary.b.long@intel.com; daryl.a.sato@intel.com
Subject: RE: Patent application P12136

Attached is the latest version of this patent application. [redacted]

Please provide your feedback as soon as possible. We're getting a lot of pressure to file the application this month.

Regards,
John

(See attached file: Patent Application v2 - P12136.doc) (See attached file: Figures - P12136.pdf)

"Brist, Gary

"Brist, Gary A" <gary.a.brist@intel.com>
"Long, Gary B"
"Sato, Daryl A"

08/27/02 03:55 PM

To: "'John_Travis@bstz.com'" <John_Travis@bstz.com>, "Brist, Gary A" <gary.a.brist@intel.com>, "Long, Gary B" <gary.b.long@intel.com>, "Sato, Daryl A" <daryl.a.sato@intel.com>
cc:
Subject: RE: Patent application P12136

John,

Attached is the word document with the proposed edits highlighted. [redacted]

Gary Brist
PCB Technologist
Materials Technology Organization

MS: AG4-409
Phone: 503.456.1246
Fax: 503.456-1223
Email: gary.a.brist@intel.com

-----Original Message-----
From: John_Travis@bstz.com [mailto:John_Travis@bstz.com]
Sent: Wednesday, August 21, 2002 1:01 PM
To: gary.a.brist@intel.com; gary.b.long@intel.com; daryl.a.sato@intel.com
Subject: RE: Patent application P12136

Have any of you had a chance to review this patent application yet?
John Travis

"Brist, Gary A" <gary.a.brist@intel.com>

08/05/02 02:05 PM

To: "'John_Travis@bstz.com'" <John_Travis@bstz.com>

cc:

Subject: RE: Your patent application P12136

John,

Apologize for not having already completed a response to you - I have been trying to manage a couple of paper deadlines the last few weeks.

I'll review and respond by Aug13th

Thanks,

Gary Brist
PCB Technologist
Materials Technology Organization

MS: AG4-409
Phone: 503.456.1246
Fax: 503.456-1223
Email: gary.a.brist@intel.com

-----Original Message-----
From: John_Travis@bstz.com [mailto:John_Travis@bstz.com]
Sent: Monday, July 22, 2002 1:37 PM
To: gary.a.brist@intel.com; gary.b.long@intel.com; daryl.a.sato@intel.com
Subject: Your patent application P12136

I have inherited the above-referenced patent application from William Ryann, who is no longer with our law firm.
Attached below is the first draft of this patent application, on which you are each listed as co-inventors. Please review and provide me with any needed corrections at your earliest convenience.

In addition to your general comments, I also need clarication on two points, which are embedded in the text in paragraphs 20 and 23 as bracketed bold text.

If you have any questions, please contact me through any of the means shown below.

Thanks,
John Travis

512-306-7644 (voice)
512-330-0476 (fax)

john_travis@bstz.com (email)

(See attached file: Patent Application v1 - P12136.doc) (See attached file: Figures - P12136.pdf)

(See attached file: P12136 Comments.ZIP)

Bob Caldwell

From: Barbara Wilson
Sent: Wednesday, January 25, 2006 11:30 AM
To: Bob Caldwell
Subject: RE: William Ryann

Yes - 6/21/2002

Barbara E. Wilson
Human Resources Manager
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
Suite 700
Los Angeles, California 90025
310.207.3800 - tel
310.207.3915 - fax

-----Original Message-----
From: Bob Caldwell
Sent: Wednesday, January 25, 2006 9:06 AM
To: Barbara Wilson
Subject: William Ryann

Hi Barbara,
I have an attorney that has asked me to find William Ryann's last day with the firm. It should be sometime around 7/02. Can you provide me with an exact date?

Thanks,

Bob